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EXAMINER	
JUNG, MICHAEL	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/588,927	ABERIN ET AL.	
	Examiner	Art Unit	
	Michael Jung	4148	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20070309*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 25 is objected to because of the following informality:

In claim 25, change "vent holes are include solder resist" to "vent holes include solder".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 33 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

35 U.S.C. 112, sixth paragraph states that a claim limitation expressed in means-plus-function language “shall be construed to cover the corresponding structure…described in the specification and equivalents thereof.” “If one employs means plus function language in a claim, one must set forth in the specification an adequate disclosure showing what is meant by that language. If an applicant fails to set forth an adequate disclosure, the applicant has in effect failed to particularly point out and distinctly claim the invention as required by the second paragraph of section 112.” In re Donaldson Co., 16 F.3d 1189, 1195, 29 USPQ2d 1845, 1850 (Fed. Cir. 1994) (in banc) (see MPEP § 2181).

The disclosure of the structure (or material or acts) may be implicit or inherent in the specification if it would have been clear to those skilled in the art what structure (or material or acts) corresponds to the means (or step)-plus-function claim limitation. See Id. at 1380, 53 USPQ2d at 1229; In re Dossel, 115 F.3d 942, 946-47, 42 USPQ2d 1881, 1885 (Fed. Cir. 1997). If there is no disclosure of structure, material or acts for performing the recited function, the claim fails to satisfy the requirements of 35 U.S.C. 112, second paragraph. Budde v. Harley-Davidson, Inc., 250 F.3d 1369, 1376, 58 USPQ2d 1801, 1806 (Fed. Cir. 2001); Cardiac Pacemakers, Inc. v. St. Jude Med., Inc., 296 F.3d 1106, 1115-18, 63 USPQ2d 1725, 1731-34 (Fed. Cir. 2002) (see MPEP § 2181)

Claim 33 in the instant case contains a limitation "means for leaving the contact area free from solder resists" that does not have corresponding structure in the specification. Nor would it have been clear to those skilled in the art what the structure (or material or acts) corresponds to the means-plus-function claim limitation as above. Therefore, the applicant has failed to particularly point out and distinctly claim the invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 23 is rejected under 35 U.S.C. 102(b) as being anticipated by US PGPub 2001/0042908 A1 to Okada et al. (hereinafter "Okada").

Regarding claim 23, Okada teaches a method to assemble a semiconductor package (Fig. 5) characterized in that the upper surface of the chip 2 and substrate 6 are covered with mold material 12 (para [0009] – "seal resin 12"; see Fig. 5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 17-21 and 24-36 are rejected under 35 U.S.C. 103(a) as being obvious over Okada in view of US 6,054,755 A to Takamichi et al. (hereinafter "Takamichi").

Regarding claim 17, Okada teaches a method comprising:

providing a substrate 6 (para [0081]) comprising a sheet of core material (para [0003] – "glass epoxy or a polyimide"), and a plurality of upper contact traces 10 (para [0081] - "electrode pad 10; Fig. 10) and upper contact pads 30 (para [0058] – "The copper plate or copper foil is patterned by etching so as to form both the electrode pads 10 and the pattern member 30; Fig. 5) on its upper surface 6A (Fig. 5);

providing external contact areas 14 on the bottom surface of the substrate 6 (para [0009] – "Additionally, the electrode pads 10 of the organic substrate 6 are electrically connected to solder balls 14, which are external connection electrodes."; see Fig. 5); and

forming a plurality of vent holes 16 in the substrate (para [0059]).

Okada neither discloses providing a second plurality of lower conducting traces and conducting vias connecting the upper conducting traces and lower conducting traces; nor covering the upper and lower surfaces of the substrate by a layer of solder resist leaving the contact areas free from solder resist.

However, Takamichi teaches providing a second plurality of lower conducting traces 45 (col. 6, ln 11-14 - "Cu-plated coat 45; Fig. 7) and conducting vias (col. 4, ln 12-15 - "through-holes") connecting the upper conducting traces (col. 4, ln 12-15 – "The wiring pattern formed on the upper side of the substrate 21…") and lower conducting traces (col. 4, ln 12-15). Takamichi also teaches covering the upper and lower surfaces of the substrate 41 (Fig. 6 and 7) by a layer of solder resist 52 (col. 6, ln 46-51) leaving the contact areas free from solder resist (col. 6, ln 46-51 – "…the portions of the wiring patterns except the connecting terminals (pads)…are covered with the solder resists films 49 and 50.").

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the method of Okada with providing a second plurality of lower conducting traces and conductive vias connecting the upper conducting traces and lower conducting traces as taught by Takamichi, so as to electrically connect the upper

conducting traces and lower conducting traces (Takamichi, col. 4, ln 12-15); and to cover the upper and lower surfaces of the plurality of vent holes as taught by Okada with the solder resist as taught by Takamichi, so as to reliably vent moisture vapor produced in a semiconductor package (Takamichi, col. 5, ln 11-22).

Regarding claim 18, Okada does not disclose the vent holes that are closed at one end by a layer of solder resist on the upper surface of the substrate.

However, Takamichi teaches the vent holes 44 that are closed at one end by a layer of solder resist 49 (col. 6, ln 46-55) on the upper surface of the substrate (Fig. 6).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the vent holes of Okada with the vent holes that are closed at one end by a layer of solder resist on the upper surface of a substrate as taught by Takamichi, so as to prevent an adhesive agent from flowing into the vent holes (Takamichi, col. 5, ln 11-14).

Regarding claim 19, Okada does not disclose the vent holes that include solder resist.

However, Takamichi teaches the vent holes 44 that include solder resist 49 (col. 6, ln 46-55; Figs. 6 and 7).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the vent holes of Okada with the vent holes that include solder resist as taught by Takamichi, so as to reliably vent moisture vapor produced in a semiconductor package (Takamichi, col. 5, ln 11-22).

Regarding claim 20, Okada teaches the vent holes 16 that are formed by drilling (para [0052]).

Regarding claim 21, Okada teaches forming the vent holes 16 in the core material 6 before a plurality of upper contact traces and upper contact pads on its upper surface, a second plurality of lower conducting traces and external contact areas on its bottom surface and depositing conducting vias (para [0052] – "…the semiconductor device shown in Fig. 5 has a plurality of vent holes (through holes) 16 previously formed in an organic substrate 6...").

Regarding claim 24, Okada teaches a substrate comprising:

a sheet of core material (para [0003] – "a typical organic substrate, there is a glass-epoxy substrate or a polyimide substrate.");

a plurality of upper contact traces 10 (para [0081] - "electrode pad 10; Fig. 10) and upper contact pads 30 (para [0058] – "The copper plate or copper foil is patterned by etching so as to form both the electrode pads 10 and the pattern member 30; Fig. 5) on its upper surface 6A (Fig. 5);

external contact areas 14 on the bottom surface of the substrate 6 (para [0009] – "Additionally, the electrode pads 10 of the organic substrate 6 are electrically connected to solder balls 14, which are external connection electrodes."; see Fig. 5); and

a plurality of vent holes 16 (para [0059]).

Okada neither discloses a second plurality of lower conducting traces and conducting vias connecting the upper conducting traces and lower conducting traces;

nor a layer of solder resists covering the upper and lower surfaces of the substrate leaving the contact areas free from solder resist.

However, Takamichi teaches a second plurality of lower conducting traces 45 (col. 6, ln 11-14 - "Cu-plated coat 45; Fig. 7) and conducting vias (col. 4, ln 12-15 - "through-holes") connecting the upper conducting traces (col. 4, ln 12-15 – "The wiring pattern formed on the upper side of the substrate 21…") and lower conducting traces (col. 4, ln 12-15). Takamichi also teaches a layer of solder resist 52 (col. 6, ln 46-51) covering the upper and lower surfaces of the substrate 41 (Fig. 6 and 7) leaving the contact areas free from solder resist (col. 6, ln 46-51 – "…the portions of the wiring patterns except the connecting terminals (pads)…are covered with the solder resists films 49 and 50.").

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the substrate having upper contact traces as taught by Okada with a second plurality of lower conducting traces and conductive vias connecting the upper conducting traces and lower conducting traces as taught by Takamichi, so as to electrically connect the upper conducting traces and lower conducting traces (Takamichi, col. 4, ln 12-15); and to modify the substrate of Okada with a layer of solder resist covering the upper and lower surfaces of the substrate leaving the contact areas free from solder resist as taught by Takamichi, so as to reliably vent moisture vapor produced in a semiconductor package (Takamichi, col. 5, ln 11-22).

Regarding claim 25, Okada does not disclose the vent holes that include solder resist.

However, Takamichi teaches the vent holes 44 that include solder resist 49 (col. 6, ln 46-55; Figs. 6 and 7).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the vent holes of Okada with the vent holes that include solder resist as taught by Takamichi, so as to reliably vent moisture vapor produced in a semiconductor package (Takamichi, col. 5, ln 11-22).

Regarding claim 26, Okada does not disclose the vent holes that are closed at one end by a layer of solder resist on the upper surface of the substrate.

However, Takamichi teaches the vent holes 44 that are closed at one end by a layer of solder resist 49 (col. 6, ln 46-55) on the upper surface of the substrate (Fig. 6).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the vent holes of Okada with the vent holes that are closed at one end by a layer of solder resist on the upper surface of a substrate as taught by Takamichi, so as to prevent an adhesive agent from flowing into the vent holes (Takamichi, col. 5, ln 11-14).

Regarding claim 27, Okada teaches the plurality of vent holes 16 (Fig. 5) that are laterally located towards the center of the substrate (Fig. 5).

Regarding claim 28, Okada teaches the plurality of vent holes 16 (Fig. 5) that are laterally located towards the center and the vent holes 16 that are located towards the outer edges of the substrate (Fig. 5).

Regarding claim 29, Okada teaches the vent holes 32 that have a diameter of approximately 1 micron to approximately 5 mm or approximately 10 micron to

approximately 0.5 mm or approximately 100 micron (para [0055] – "…the diameter of the small hole 32 is made about 50 micron…").

Regarding claim 30, Okada teaches a semiconductor package comprising:

a sheet of core material (para [0003] – "a typical organic substrate, there is a glass-epoxy substrate or a polyimide substrate.");

a plurality of upper contact traces 10 (para [0081] - "electrode pad 10; Fig. 10) and upper contact pads 30 (para [0058] – "The copper plate or copper foil is patterned by etching so as to form both the electrode pads 10 and the pattern member 30; Fig. 5) on its upper surface 6A (Fig. 5);

an external contact areas on its bottom surface (para [0009] – "Additionally, the electrode pads 10 of the organic substrate 6 are electrically connected to solder balls 14, which are external connection electrodes...")

a plurality of vent holes 16 (para [0059]);

a substrate 6 (para [0081]); and

a semiconductor chip 2 including an active surface (para [0081] – "semiconductor chip 2, which is mounted to the substrate by a flip chip mounting method.") including a plurality of chip contact areas (Figs. 3 and10 show a plurality of stud electrodes bonded to the electrode pads 10; para [0012]), electrically connected to the substrate (para [0012] – "Additionally, the electrode pad 10 of the organic substrate 6 is electrically connected to the solder balls 14, which are external connection electrodes, via the circuit pattern formed on the organic substrate 6.").

Okada neither discloses a second plurality of lower conducting traces and conducting vias connecting the upper conducting traces and lower conducting traces; nor a layer of solder resists covering the upper and lower surfaces of the substrate leaving the contact areas free from solder resist.

However, Takamichi teaches a second plurality of lower conducting traces 45 (col. 6, ln 11-14 - "Cu-plated coat 45; Fig. 7) and conducting vias (col. 4, ln 12-15 - "through-holes") connecting the upper conducting traces (col. 4, ln 12-15 – "The wiring pattern formed on the upper side of the substrate 21…") and lower conducting traces (col. 4, ln 12-15). Takamichi also teaches a layer of solder resist 52 (col. 6, ln 46-51) covering the upper and lower surfaces of the substrate 41 (Fig. 6 and 7) leaving the contact areas free from solder resist (col. 6, ln 46-51 – "…the portions of the wiring patterns except the connecting terminals (pads)…are covered with the solder resists films 49 and 50.").

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the substrate having upper contact traces as taught by Okada with a second plurality of lower conducting traces and conductive vias connecting the upper conducting traces and lower conducting traces as taught by Takamichi, so as to electrically connect the upper conducting traces and lower conducting traces (Takamichi, col. 4, ln 12-15); and to modify the substrate of Okada with a layer of solder resist covering the upper and lower surfaces of the substrate leaving the contact areas free from solder resist as taught by Takamichi, so as to reliably vent moisture vapor produced in a semiconductor package (Takamichi, col. 5, ln 11-22).

Regarding claim 31, Okada teaches the chip 2 (Fig. 5) that is encapsulated by mold material 12 (para [0009]).

Regarding claim 32, Okada teaches the chip that is mounted to the substrate by the flip-chip technique (para [0081]).

Regarding claim 33, Okada teaches a substrate for a semiconductor package comprising:

sheet of core material (para [0003] – "a typical organic substrate, there is a glass-epoxy substrate or a polyimide substrate.") with an upper surface and a bottom surface (Fig. 5);

a plurality of upper contact traces 10 (para [0081] - "electrode pad 10; Fig. 10) and upper contact pads 30 (para [0058] – "The copper plate or copper foil is patterned by etching so as to form both the electrode pads 10 and the pattern member 30; Fig. 5) on its upper surface 6A (Fig. 5);

external contact areas 14 on the bottom surface of the substrate 6 (para [0009] – "Additionally, the electrode pads 10 of the organic substrate 6 are electrically connected to solder balls 14, which are external connection electrodes."; see Fig. 5); and

a plurality of vent holes 16 (para [0059]).

Okada does not disclose the sheet of core material with the upper surface and the bottom surface each covered with a layer of solder resist; a means for leaving the contact areas free from solder resists; or a plurality of bottom conducting traces and a plurality of conducting vias connecting the upper conducting traces and the bottom conducting traces.

However, Takamichi teaches a sheet of core material 41 (col. 6, ln 46-51) with an upper surface and a bottom surface each covered with a layer of solder resist 49, 52 (col. 6, ln 46-51, Figs. 6 and 7) and a means for leaving the contact areas free from solder resist (col. 6, ln 46-51 – "…the portions of the wiring patterns except the connecting terminals (pads)…are covered with the solder resists films 49 and 50.").

Takamichi also teaches a plurality of bottom conducting traces 45 (col. 6, ln 11-14 - "Cu-plated coated 45; Fig. 7) and conducting vias (col. 4, ln 12-15 - "through-holes") connecting the upper conducting traces (col. 4, ln 12-15 – "The wiring pattern formed on the upper side of the substrate 21…") and bottom conducting traces (col. 4, ln 12-15).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the substrate of Okada with a layer of solder resists that covers the upper surface and the bottom surface of the sheet of core material while leaving the contact areas free from solder resist as taught by Takamichi, so as to reliably vent moisture vapor produced in a semiconductor package (Takamichi, col. 5, ln 11-22); and to modify the substrate having upper contact traces as taught by Okada with a plurality of bottom conducting traces and conducting vias connecting the upper conducting traces and bottom conducting traces as taught by Takamichi to the, so as to electrically connect the upper conducting traces and bottom conducting traces (Takamichi, col. 4, ln 12-15).

Regarding claim 34, Okada does not disclose the vent holes that include solder resist.

However, Takamichi teaches the vent holes 44 that include solder resist 49 (col. 6, ln 46-55; Figs. 6 and 7).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the vent holes of Okada with the vent holes that include solder resist as taught by Takamichi, so as to reliably vent moisture vapor produced in a semiconductor package (Takamichi, col. 5, ln 11-22).

Regarding claim 35, Okada does not disclose the vent holes that are closed at one end by a layer of solder resist on the upper surface of the substrate.

However, Takamichi teaches the vent holes 44 that are closed at one end by a layer of solder resist 49 (col. 6, ln 46-55) on the upper surface of the substrate (Fig. 6).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the vent holes of Okada with the vent holes that are closed at one end by a layer of solder resist on the upper surface of a substrate as taught by Takamichi, so as to prevent an adhesive agent from flowing into the vent holes (Takamichi, col. 5, ln 11-14).

Regarding claim 36, Okada teaches the plurality of vent holes 16 (Fig. 5) that are laterally located towards the center of the substrate (Fig. 5).

5. Claim 22 is rejected under 35 U.S.C. 103(a) as being obvious over Okada in view of Takamichi, and further in view of US PGPub 2002/0043721 A1 to Weber.

Regarding claim 22, Okada teaches a method to assemble a semiconductor package comprising:

providing a substrate 6 (para [0081]) comprising a sheet of core material (para [0003] – "glass epoxy or a polyimide") and a plurality of upper contact traces 10 (para [0081] - "electrode pad 10; Fig. 10) and upper contact pads 30 (para [0058] – "The copper plate or copper foil is patterned by etching so as to form both the electrode pads 10 and the pattern member 30; Fig. 5) on its upper surface 6A (Fig. 5);

providing external contact areas 14 on the bottom surface of the substrate 6 (para [0009] – "Additionally, the electrode pads 10 of the organic substrate 6 are electrically connected to solder balls 14, which are external connection electrodes."; see Fig. 5);

forming a plurality of vent holes 16 in the substrate (para [0059]);

providing a semiconductor chip 2 (para [0081]) comprising an active surface (para [0081] – "semiconductor chip 2, which is mounted to the substrate by a flip chip mounting method.") including a plurality of chip contact areas (Figs. 3 and10 show a plurality of stud electrodes bonded to the electrode pads 10; para [0012]);

mounting the chip 2 on the upper surface of the redistribution board 6 by microscopic solder balls 20 (para [0012] – "bonding stud electrodes 20") between the chip contacts and upper contact areas 10 (Figs. 3 and 10 show electrical contacts 10 above and below the bonding stud electrodes 20); and

underfilling the area between the chip 2 and the upper surface of the redistribution board 6a with epoxy resin 4 (para [0056] – "adhesive 4"; see para [0019] – "…underfill material is cured…").

Okada neither discloses providing a second plurality of lower conducting traces and a plurality of conducting vias connecting the upper conducting traces and lower conducting traces; nor covering the upper and lower surfaces of the substrate by a layer of solder resist leaving the contact areas free from solder resists.

However, Takamichi teaches providing a second plurality of lower conducting traces 45 (col. 6, ln 11-14 - "Cu-plated coat 45; see Fig. 7) and a plurality of conducting vias (col. 4, ln 12-15 - "through-holes") connecting the upper conducting traces (col. 4, ln 12-15 – "The wiring pattern formed on the upper side of the substrate 21…") and lower conducting traces (col. 4, ln 12-15). Takamichi also teaches covering the upper and lower surfaces of the substrate 41 (Fig. 6 and 7) by a layer of solder resist 52 (col. 6, ln 46-51) leaving the contact areas free from solder resist (col. 6, ln 46-51 – "…the portions of the wiring patterns except the connecting terminals (pads)…are covered with the solder resists films 49 and 50.").

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the method of Okada with providing a second plurality of lower conducting traces and conductive vias connecting the upper conducting traces and lower conducting traces as taught by Takamichi, so as to electrically connect the upper conducting traces and lower conducting traces (Takamichi, col. 4, ln 12-15); and to cover the upper and lower surfaces of the plurality of vent holes as taught by Okada with the solder resist as taught by Takamichi, so as to reliably vent moisture vapor produced in a semiconductor package (Takamichi, col. 5, ln 11-22).

Neither Okada nor Takamichi discloses performing a solder reflow.

However, Weber teaches performing a solder reflow (para [0008]).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to modify mounting the chip on the upper surface of the redistribution board by microscopic solder balls between the chip contact and upper contact areas as taught by the combination of Okada and Takamichi with performing a solder reflow as taught by Weber, so as to provide an electrical contact between the solder bumps and the circuit traces (Weber, para [0008]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Jung whose telephone number is (571) 270-3345. The examiner can normally be reached on Mondays through Fridays from 7:30 AM to 5:00 PM EST. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anh Mai can be reached on (571) 272-1995. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael Jung/
Examiner, Art Unit 4148
13 April 2009

/Scott B. Geyer/
Supervisory Patent Examiner, Art Unit 4148